MJF3055 (NPN), MJF2955 (PNP)

Complementary Silicon Power Transistors

Specifically designed for general purpose amplifier and switching applications.

Features

- Isolated Overmold Package (1500 Volts RMS Min)
- Electrically Similar to the Popular MJE3055T and MJE2955T
- Collector−Emitter Sustaining Voltage − $V_{CEO(sus)}$ 90 Volts
- 10 Amperes Rated Collector Current
- No Isolating Washers Required
- Reduced System Cost
- UL Recognized, File #E69369, to 3500 V_{RMS} Isolation
- Epoxy Meets UL 94 V−0 at 0.125 in
- ESD Ratings: Machine Model, C; > 400 V
  Human Body Model, 3B; > 8000 V
- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Sustaining Voltage	$V_{CEO(sus)}$	90	Vdc
Collector−Emitter Breakdown Voltage	V_{CES}	90	Vdc
Base−Emitter Voltage	V_{EBO}	5.0	Vdc
Collector Current − Continuous	I_C	10	Adc
Base Current − Continuous	I_B	6.0	Adc
RMS Isolation Voltage (Note 3) (t = 0.3 sec, R.H. ≤ 30%, T_A = 25°C) Per Figure 5	V_{ISOL}	4500	V_{RMS}
Total Power Dissipation @ T_C = 25°C (Note 2) Derate above 25°C	P_D	30 0.25	W W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	2.0 0.016	W W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case (Note 2)	$R_{\theta JC}$	4.0	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	62.5	°C/W
Lead Temperature for Soldering Purposes	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.
2. Measurement made with thermocouple contacting the bottom insulated surface (in a location beneath the die), the devices mounted on a heatsink with thermal grease and a mounting torque of ≥ 6 in. lbs.
3. Proper strike and creepage distance must be provided.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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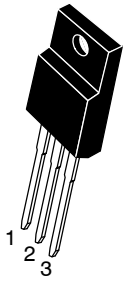
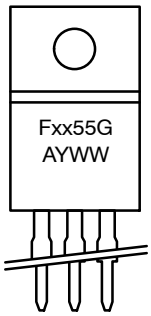
COMPLEMENTARY SILICON POWER TRANSISTORS 10 AMPERES 90 VOLTS, 30 WATTS



TO−220 FULLPACK CASE 221D STYLE 2

MARKING DIAGRAM



Fxx55 = Specific Device Code
xx= 29 or 30
G = Pb−Free Package
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MJF2955	TO−220 FULLPACK	50 Units/Rail
MJF2955G	TO−220 FULLPACK (Pb−Free)	50 Units/Rail
MJF3055	TO−220 FULLPACK	50 Units/Rail
MJF3055G	TO−220 FULLPACK (Pb−Free)	50 Units/Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS (Note 4)				
Collector−Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	90	−	Vdc
Collector Cutoff Current (V_{CE} = 90 Vdc, V_{BE} = 0)	I_{CES}	−	1.0	μAdc
Collector Cutoff Current (V_{CE} = 90 Vdc, I_E = 0)	I_{CBO}	−	1.0	μAdc
Emitter−Base Leakage (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	−	1.0	μAdc
ON CHARACTERISTICS (Note 4)				
DC Current Gain (I_{CE} = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_{CE} = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	100 −	−
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	 − −	 1.0 2.5	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{BE} = 4.0 Vdc)	$V_{BE(on)}$	−	1.5	Vdc
DYNAMIC CHARACTERISTICS				
Current−Gain−Bandwidth Product (V_{CE} = 10 Vdc, I_C = 0.5 Adc, f_{test} = 500 kHz)	f_T	2.0	−	MHz

4. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle ≤ 10%.

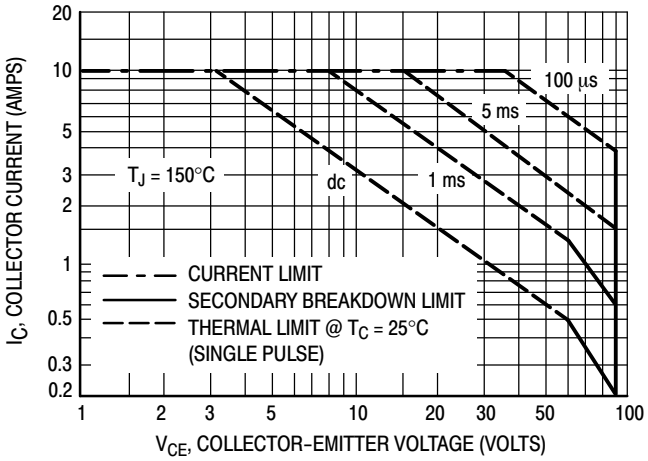


Figure 1. Maximum Forward Bias Safe Operating Area

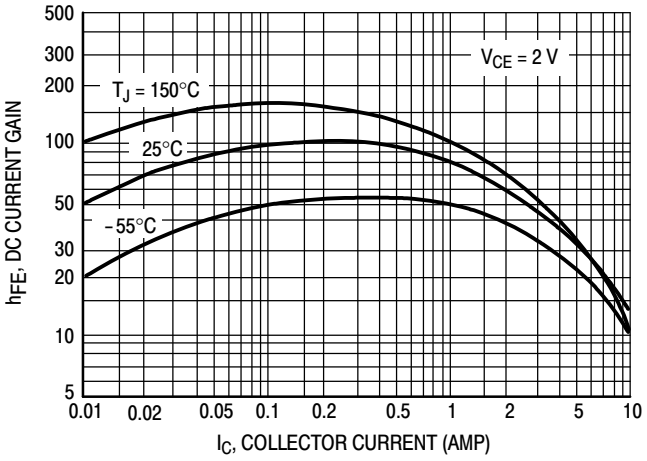


Figure 2. DC Current Gain

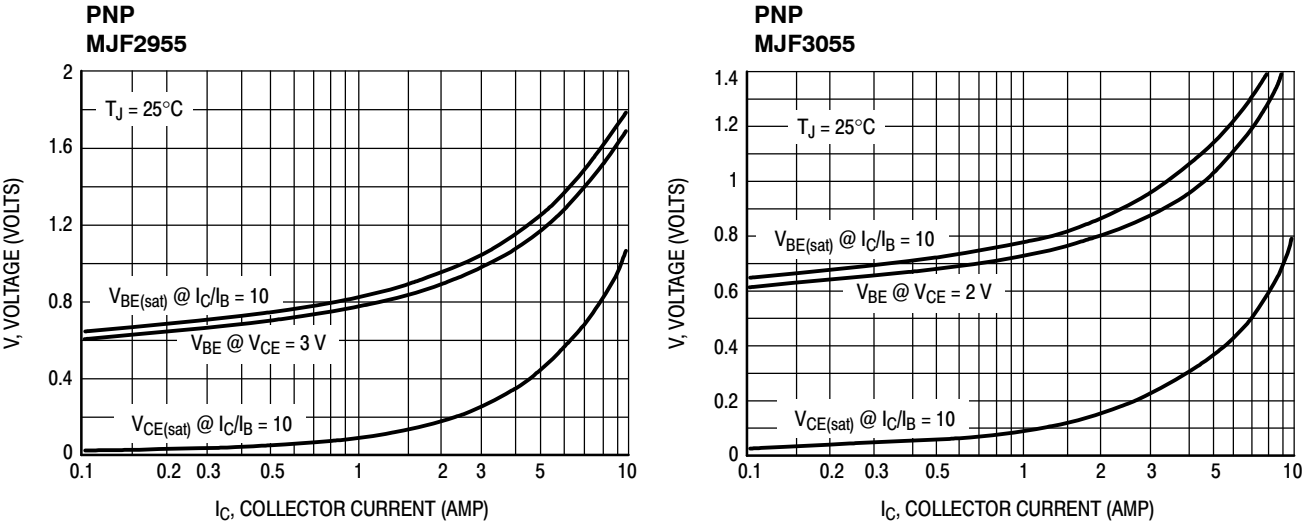


Figure 3. “On” Voltages

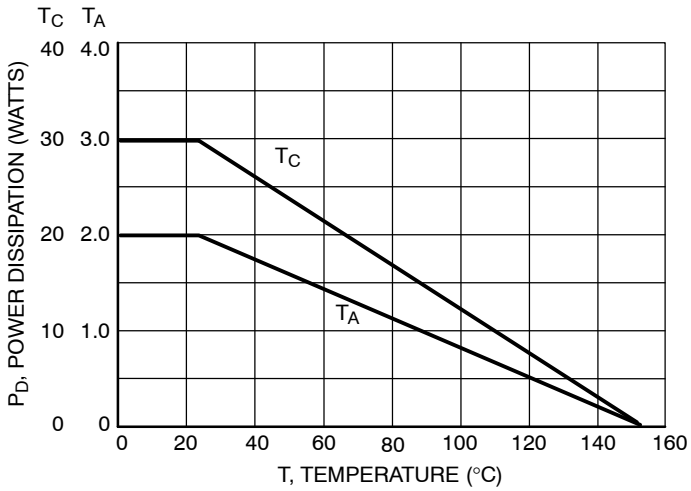


Figure 4. Power Derating

TEST CONDITIONS FOR ISOLATION TESTS*

FULLY ISOLATED PACKAGE

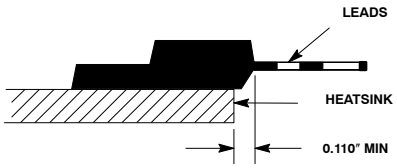


Figure 5. Mounting Position

*Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION

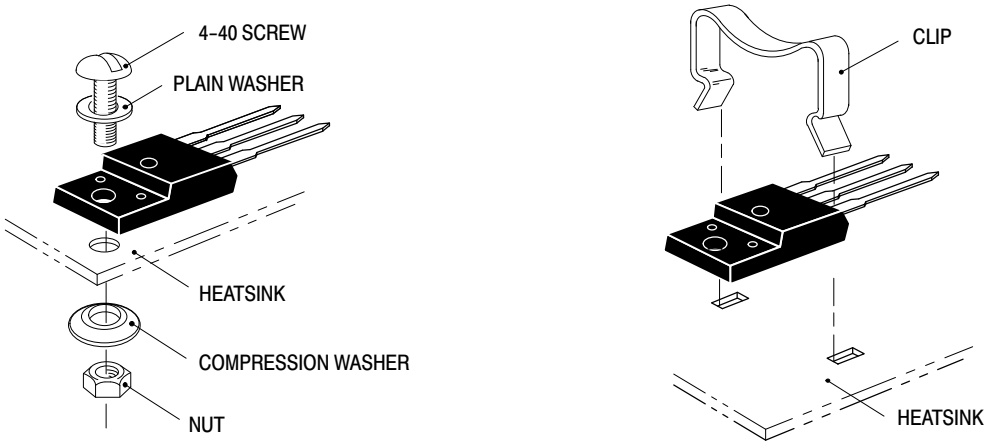


Figure 6. Typical Mounting Techniques*

Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in · lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

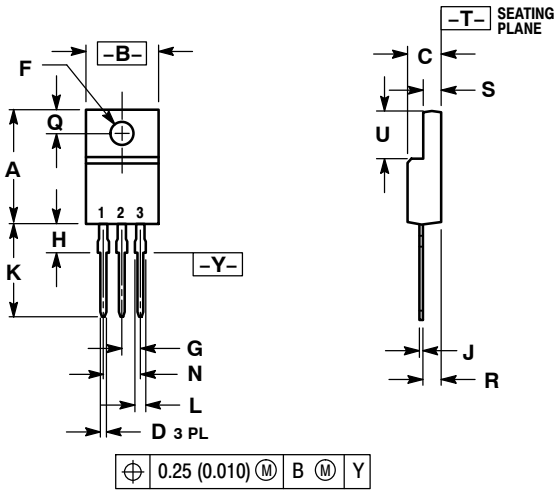
Destructive laboratory tests show that using a hex head 4−40 screw, without washers, and applying a torque in excess of 20 in · lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4−40 screws indicate that the screw slot fails between 15 to 20 in · lbs without adversely affecting the package. However, in order to positively ensure the package integrity of the fully isolated device, ON Semiconductor does not recommend exceeding 10 in · lbs of mounting torque under any mounting conditions.

** For more information about mounting power semiconductors see Application Note AN1040.

PACKAGE DIMENSIONS

TO−220 FULLPAK
CASE 221D−03
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH
3. 221D−01 THRU 221D−02 OBSOLETE, NEW STANDARD 221D−03.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.617	0.635	15.67	16.12
B	0.392	0.419	9.96	10.63
C	0.177	0.193	4.50	4.90
D	0.024	0.039	0.60	1.00
F	0.116	0.129	2.95	3.28
G	0.100 BSC		2.54 BSC	
H	0.118	0.135	3.00	3.43
J	0.018	0.025	0.45	0.63
K	0.503	0.541	12.78	13.73
L	0.048	0.058	1.23	1.47
N	0.200 BSC		5.08 BSC	
Q	0.122	0.138	3.10	3.50
R	0.099	0.117	2.51	2.96
S	0.092	0.113	2.34	2.87
U	0.239	0.271	6.06	6.88

STYLE 2:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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